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Oscillations of hopping conductance in an array of charge-tunable self-assembled quantum dots

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Abstract. An array of 3×10^7 Ge self-assembled quantum dots is embedded into the active channel of a Si metal–oxide field-effect transistor. Conductance oscillations with the gate voltage resulting from successive loading of holes into the dots are observed. On the basis of measurements of the temperature dependence of the conductance maxima, the charge-transfer mechanism in the channel is identified as being due to variable-range hopping between the dots, with the typical hopping energy determined by inter-dot Coulomb interaction. The characteristic spatial dimension of the hole wavefunctions as well as the charging energies of the dots are determined from the conductance data.

In a single quantum dot (QD) weakly coupled by tunnelling barriers to two leads, the interplay of single-electron charging effects and resonant tunnelling through quantized states leads to conductance oscillations as the electrochemical potential of the dot is tuned [1]. This phenomenon underlies the working of nanoscale single-electron transistors which have a number of practical uses, ranging from metrology to computing. Recently, research has focused on the double-dot systems [2] whose behaviour is found to be mainly affected by electrostatic coupling between the two dots inside the artificial molecule. The next step is to create and study large arrays of QDs in close proximity, allowing Coulomb interaction and tunnelling between them [3]. Such systems can be considered as potential electronic networks for quantum computers [4], and therefore may be particularly valuable in future high-power digital processors. The behaviour of a multi-dot structure is expected to be more complicated for several reasons: (i) the QDs are inevitably not sufficiently identical in size, and that can cause smearing of their atomic-like properties; (ii) in contrast to the case for a single dot, the interaction of the dots in an ensemble can be significant; (iii) transport through the system may be dominated by thermally assisted hopping between the dots rather than by resonant tunnelling. Thus, a key question to be answered is that of whether there can be conductance oscillations in large arrays of QDs.

In a previous paper [5], we have reported measurements of hopping transport in a modulation-doped Si field-effect structure with a layer of Ge QDs embedded in proximity with the p-type conductive channel. At low temperatures ($T \simeq 6$ K), a small ($\sim$10–20%) contribution to the conductance which intriguingly oscillated with the gate voltage was detected and was ascribed to direct hopping of holes between dots. In the work reported in this article, we studied a new device, which contains of about 3×10^7 QDs and shows conductance oscillations

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at $T \leqslant 100$ K. For the first time, we have been able to study the temperature dependence of the conductance maxima and to demonstrate that charge transport in the channel proceeds by hole variable-range hopping between the dots and is distinctly affected by the inter-dot Coulomb correlations.

Silicon-on-insulator films prepared from a SIMOX wafer (p-type Si substrate, 400 nm buried SiO_2 and 170 nm top Si layer) were used for fabricating the metal–oxide–semiconductor field-effect transistor (MOSFET) structures (see figure 1). The channel was a quantum dot layer grown by molecular-beam epitaxy of Ge on Si(001) in the Stranski–Krastanov growth mode. This produces spontaneous formation (self-assembling) of Ge nanoclusters (quantum dots) randomly distributed in the plane [5–7]. From STM measurements, the areal density of the dots was estimated to be $n_{QD} = 3 \times 10^{15}$ m^{-2}. The average size of the dot base length is found around 15 nm, the height is ≈ 1.5 nm, and the dot uniformity is about 20%. The structure was then capped with 40 nm of i-Si. The channel was patterned by photolithography to form a Si island of 100 μm width and 108 μm length, etched down to the underlying SiO_2. Source and drain electrodes were made using Al evaporation and annealing at 450 °C in a N_2 atmosphere. A plasma-enhanced chemical-vapour-deposition oxide of 60 nm thickness was deposited as the gate insulator and, finally, a square-shaped (100×100 μm^2) Al gate was deposited. The drain current (I_d) as a function of the gate voltage (V_g) was measured in the temperature range from 300 K to 4.2 K with the drain voltage fixed at $V_d = 100$ mV which ensured ohmic conduction at all experimental temperatures.

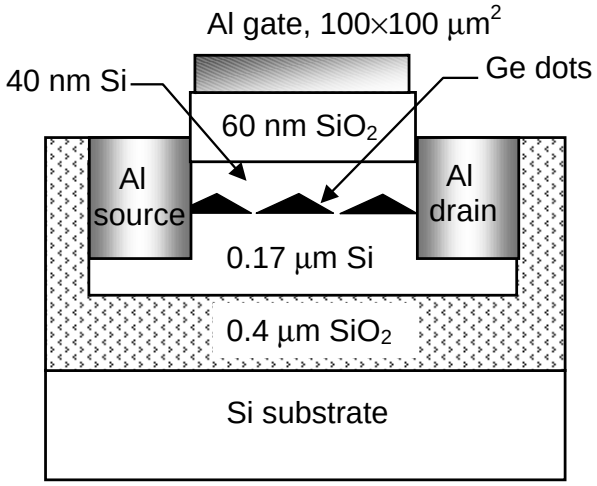

Figure 1. A schematic diagram of the sample structure.

The channel conductance ($G \equiv I_d/V_d$) versus the gate voltage is depicted in linear and semilogarithmic plots in figure 2. At room temperature, the G–V_g characteristic shows a shoulder which evolves into a broad conductance peak in the voltage range from 2 V to 6 V as the temperature decreases. In order to analyse the peak's structure, we subtract the smoothly varying background (see below). After the background is subtracted, the conductance modulation can be very well described by a sum of four Gaussian peaks. Figure 3 demonstrates the result of decomposition of the various experimental curves into four Gaussians, labelled as QD6, QD5, QD4, and QD3†. The position of those peaks as a function of temperature is

† We label the dot states in terms of the number of holes in each dot. For example, the peak observed at $V_g \approx 5.5$ V is labelled QD3 because it corresponds to loading of the third hole into the dots, this hole entering the first of the excited states with the two ground-state levels already fully occupied. The peak corresponds to a mean loading of 5/2 holes per dot.

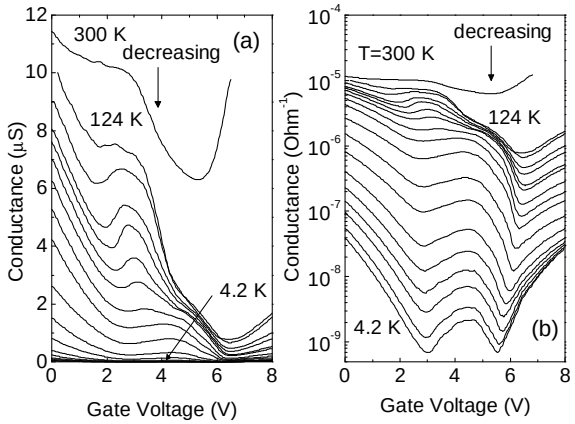

Figure 2. Channel conductance versus gate voltage characteristics shown in linear (a) and semi-logarithmic (b) plots. The source–drain voltage is 100 mV. The temperature decreases from top to bottom.

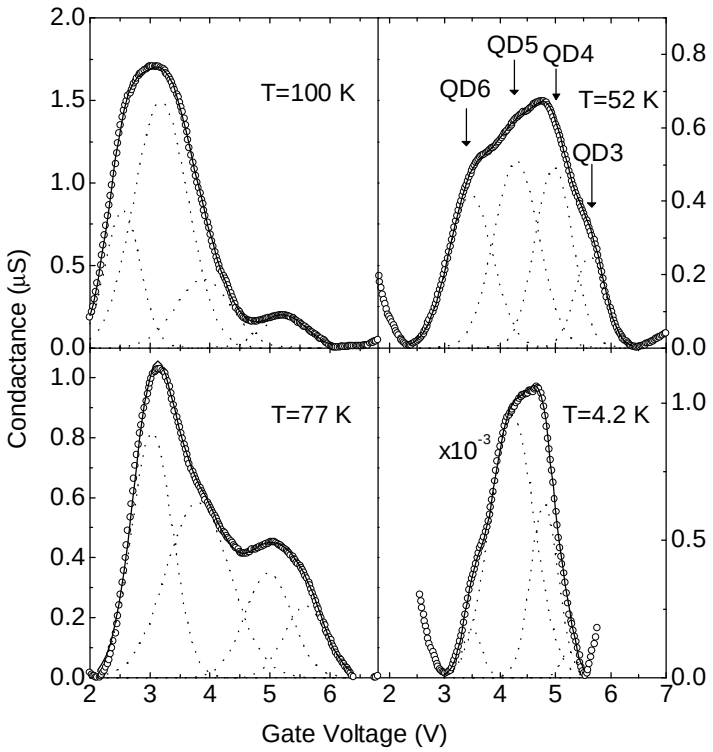

Figure 3. Dot conductance versus gate potential for four temperatures. Circles show the experimental data with the background subtracted; solid lines give the result of decomposition into Gaussians.

displayed in figure 4. Clearly, the fourfold structure with a gate voltage separation $\Delta V_g \approx 0.7\,\mathrm{V}$ between the peaks is well defined and completely reproducible over the whole temperature range. Very similar fine structure consistent with four maxima has been observed by us in the

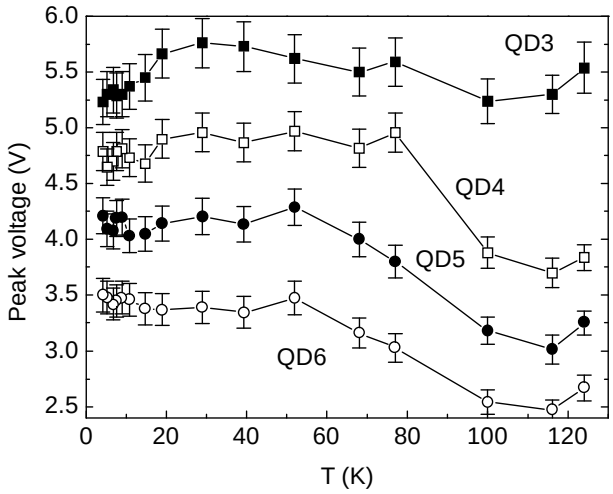

Figure 4. The position of the peaks in figure 3 as a function of temperature.

admittance spectra of Si-based Schottky diodes with Ge quantum dots [8] and ascribed to the individual charging of the fourfold-degenerate first excited state in the Ge nanoclusters. The average energy splitting due to on-site hole correlation or charging energy was found to be $\Delta E = 29 \pm 16$ meV [8].

To demonstrate that the observed conductance peaks come from charging of the quantum dots, we first estimate the charge density induced by the change in the gate voltage ΔV_g and compared this quantity with the density of QDs. A change of gate potential ΔV_g induces a change Δn in the two-dimensional carrier density given by $\Delta n = C_g \, \Delta V_g / e$, where C_g is the capacitance per unit area between the gate and the dot layer, e is the electron charge. Taking the geometrical parameters of the gate, relative permittivity $\epsilon = 3.9$ for SiO_2, $\Delta V_g = 0.7$ V for the separation of successive peaks, and supposing the electrostatic fields to be one-dimensional, we find $C_g = 4.7 \times 10^{-4}$ F m^{-2} and $\Delta n \approx 2.1 \times 10^{15}$ m^{-2}. The latter value is consistent with the density of quantum dots, $n_{QD} = 3 \times 10^{15}$ m^{-2}, strongly supporting the interpretation that each constituent conductance peak originates from loading of *one hole* into each dot. The maximum conductivity occurs when the given level is half-filled as this maximizes the product of possible initial and final states for the tunnelling process that avoids increasing the on-site correlation energy.

The above analysis can be checked by using C–V measurements to verify the electrostatics necessary for charging of the dots. We measured the capacitance between the source and drain connected together and the gate. Remember that the source and drain contact the underlying Si. The 100 kHz C–V_g characteristics at $T = 300$ K and at 4.2 K are shown in figure 5. The capacitance falls with increasing V_g corresponding to the increasing depletion layer thickness in the Si below the gate oxide. At 4.2 K, we see, superimposed on the falling capacitance, structure in the 3–6 V range associated with filling of the p states and also structure in the 8–9.5 V range which we attribute to filling of the s states. We may use values of C_g together with the acceptor concentration in the Si, $N_B = 7 \times 10^{22}$ m^{-3} (determined by Hall measurements), to estimate the electrostatic configuration at various values of V_g. At $V_g = 9.5$ V, just before the filling of the ground-state levels, $C_g \approx 3.4$ pF which corresponds to the depletion layer extending to some 88 nm below the dot layer. The corresponding band bending between the deep Si and the dot layer is 414 mV. Just before the extended states start to fill, $C_g \approx 3.7$ pF and the depletion

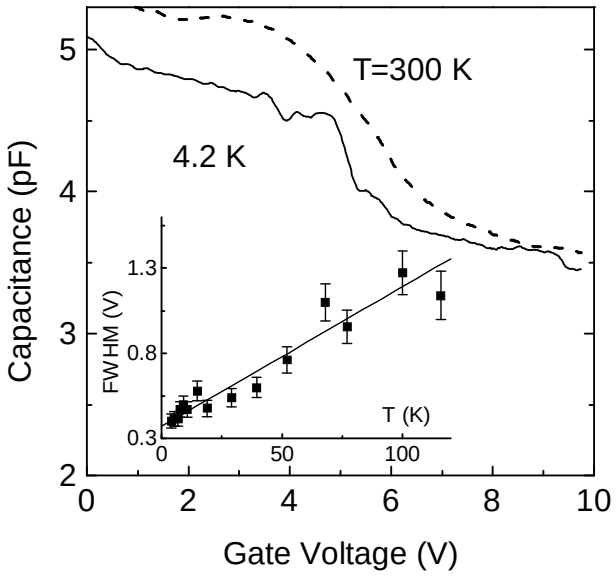

Figure 5. Capacitance–voltage characteristics. The capacitance was measured between the source and drain joined together and the gate. Values have been corrected for an estimated stray capacitance of about 0.7 pF. Inset: the temperature dependence of the FWHM of the QD3 peak in figure 3 with a linear fit to the data.

thickness below the dot layer is 62 nm with a corresponding band bending of 220 mV. These simplistic results are compatible with the known Si–Ge valence band offset and the expected energies of the hole bound states [9]. After the excited states are filled, $C_g \approx 4.7$ pF implying that the effective boundary of the depletion region is now at the dot layer. The depletion layer thickness d_d then continues to fall as V_g is decreased. At $V_g = 0$ V, $d_d = 23$ nm and the dot layer is about 17 nm into the unperturbed Si. The capacitance measurements are thus consistent with our interpretation of the conductivity results.

At large positive V_g, capacitance only decreases weakly with increasing gate voltage, in contrast to the conductance which shows a strong rise (see figure 2). Separate measurements confirm that in this region leakage current through the insulator becomes comparable with the source–drain current. Therefore we conclude that the apparent increase of background conductance at $V_g > 6$ V is a result of leakage through the gate SiO_2.

The energy level separation (ΔE) of the different charge states in the dots can be estimated by using $\Delta E = \eta e\, \Delta V_g$, where the gate modulation coefficient η relates the gate voltage to the hole energy inside the dot. This coefficient can be determined in two ways. One way is to calculate η from the temperature dependence of the full width at half-maximum (FWHM) of the conductance peaks which, for a single dot showing Coulomb blockade oscillations, should be broadened with T as $3.5k_BT/(\eta e)$ [10] (k_B is Boltzmann's constant). By measuring the FWHM of the peak QD3 as a function of temperature (figure 5), we obtain $\eta = 3.4 \times 10^{-2}$ with a residual FWHM of about 0.37 V which is a result of statistical fluctuation in the dot ensemble. Another way of calculating η has been proposed in [5]. When most of the charge induced by a change of gate voltage, ΔV_g, is captured by the QDs as discussed above, then the change in potential of the dot is given by $\Delta\phi = e\,\Delta n/C_{QD} = C_g\,\Delta V_g/(n_{QD}C_{QD})$, where C_{QD} is the dot self-capacitance. Thus $\eta = \Delta\phi/\Delta V_g = C_g/(n_{QD}C_{QD})$. The value of C_{QD} for a disc-shaped dot with diameter D in classical electrostatics is given by $C_{QD} = 4\epsilon\epsilon_0 D$. For

$D = 15$ nm and $\epsilon = \epsilon_{\rm Si} = 11.7$, this yields $C_{QD} = 5.5$ aF and $\eta = 3.5 \times 10^{-2}$. Obviously, the agreement between the two above estimates of the gate voltage–dot energy modulation coefficient is very satisfactory. The estimated charging energy, based on these calculations, is about 23 meV. Again, this value is consistent with our previous admittance experiments [8].

We may ask why we do not observe conductance maxima associated with filling of the hole ground states (QD1 and QD2 maxima) as we did with our earlier structures [5]. The probable explanation is that the gate leakage current at $V_g \approx 9$ V, where the capacitance measurements show the s states to be filling, prevents sufficient accuracy for measurement of hopping conductivity through the s levels, which is expected to be smaller as a result of the reduced localization length of the wavefunctions.

A useful way to identify the mechanism of carrier transport is to study the temperature dependence of the conductance. In the regime of resonant tunnelling through discrete energy levels, conductivity depends weakly on temperature. The current peak height should increase as the temperature is reduced due to diminished thermal broadening of the resonance. In contrast, hopping conduction is thermally activated and usually described by

$$G(T) = G_0 \exp[-(T_0/T)^x] \tag{1}$$

where, in the two-dimensional case and in the absence of long-range Coulomb interaction, the exponent $x = 1/3$ and $T_0 \propto [g(E_F)\ell^3]^{-1}$, $g(E_F)$ being the density of states in the vicinity of the Fermi level E_F and ℓ the localization length. When the Coulomb interaction between charges localized on remote centres is significant, $G(T)$ should follow a different dependence with $x = 1/2$ and $T_0 \propto e^2/\epsilon_0\epsilon\ell$ [11]. Figure 6 shows the temperature dependence of the four conductance peaks, QD3–QD6. For all maxima (symbols) we see a temperature-dependent activation energy reminiscent of variable-range hopping. A best fit to these curves (dotted lines) indicates that below 100 K the temperature dependence can be described by equation (1) with $x \simeq 0.5$ and $T_0 = 395$–565 K (see table 1).

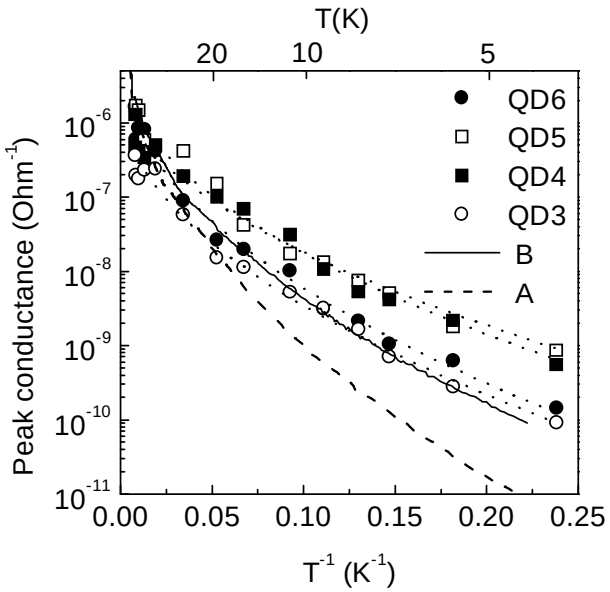

Figure 6. The temperature dependence of the conductance maxima (symbols). Dotted lines are the best fit of the experimental data to equation (1). Broken and solid lines represent the temperature dependence of the conductance in the test samples A and B, respectively (see the text).

Table 1. Fitting parameters for the variable-range-hopping conduction through the quantum dots.

Conductance maximum	x	T_0 (K)	ℓ (nm)
QD6	0.49 ± 0.11	565 ± 58	15.4 ± 1.6
QD5	0.49 ± 0.14	395 ± 48	21.4 ± 3.1
QD4	0.51 ± 0.14	405 ± 49	21.1 ± 2.2
QD3	0.51 ± 0.10	536 ± 52	16.2 ± 1.5
Sample A	0.50 ± 0.01	1176 ± 36	7.6 ± 0.2
Sample B	0.51 ± 0.01	581 ± 37	15.0 ± 0.9

We can check the hopping model for our structure and extract a value of the localization radius ℓ by making a quantitative comparison with the theoretical prediction. With $k_B T_0 = 6.2e^2/(4\pi\epsilon\epsilon_0\ell)$ [11] the spatial dimension of the wavefunctions is found to be $\ell = 15$–21 nm (table 1). For variable-range tunnelling to be occurring, the temperature-dependent optimum hop distance $R_{opt} = 0.25\ell(T_0/T)^{1/2}$ must be larger than both the localization length and the inter-dot distance (3–4 nm). At $T = 10$ K and with $T_0 = 395$–565 K, we have $R_{opt} = 29$–34 nm. Therefore these conditions are satisfied.

To obtain further evidence to support a hopping mechanism in the MOSFET, we have fabricated two test samples without any oxides or gate. Both samples contain a remotely doped layer of Ge QDs grown on a semi-insulating Si(001) substrate. In sample A the doping level is such that only the ground state contains holes, there being 3/2 holes per dot taken from impurities, while in sample B, the ground state is full and the first excited state is partially occupied with a total of 5/2 holes per dot. The results of $G(T)$ measurements for the two samples are shown in figure 6 by solid and broken lines, respectively. For both samples, best fits again give $x \simeq 0.5$, with $T_0 = 1176$ K for sample A† and $T_0 = 581$ K for sample B. The latter is close to the value found for the corresponding state (QD3) in the MOSFET structure (see table 1). Moreover, the actual values of $G(T)$ for sample B match the temperature dependence of conductance maximum QD3. These results provide strong support for the assertion that the observed conductance oscillations do originate from hopping of holes through the discrete energy levels of the first excited state.

In summary, we have described a set of experiments in which we have studied hopping transport in a field-effect transistor containing some 3×10^7 quantum dots. We demonstrate that below ∼100 K this system is able to show conductance oscillations associated with single-electron charging of each dot. From the temperature dependence of conductance maxima, we identify the conduction mechanism as variable-range hopping in a density of states determined by Coulomb interaction between the dots.

Acknowledgments

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† The characteristic length of the ground state turns out to be less than that of the excited state by a factor of 2–3. This is consistent with our previous magnetoresistance measurements [5].

References

[1] For a review, see Grabert H and Devoret M H (ed) 1991 *Single-Charge Tunneling—Coulomb Blockade Phenomena in Nanostructures (NATO ASI Series B: Physics)* (New York: Plenum)

[2] Hofmann F, Heinzel T, Wharam D A, Kotthaus J P, Böhm G, Klein W, Tränke G and Weimann G 1995 *Phys. Rev.* B **51** 13 872
Dixon D, Kouwenhoven L P, McEuen P L, Nagamune Y, Motohisa J and Sakaki H 1996 *Phys. Rev.* B **53** 12 625
Blick R H, Haug R J, Weis J, Pfannkuche D, von Klitzing K and Eberl K 1996 *Phys. Rev.* B **53** 7899
Haug R J, Weis J, Blick R H, von Klitzing K, Berl K and Ploog K 1996 *Semicond. Sci. Technol.* **11** 381
Blick R H, Schmidt T, Haug R and von Klitzing K 1996 *Semicond. Sci. Technol.* **11** 1506
Schmidt T, Haug R J, von Klitzing K, Förster A and Lüth H 1997 *Phys. Rev. Lett.* **78** 1544

[3] Duruöz C I, Clarke R M, Marcus C M and Harris J S Jr 1995 *Phys. Rev. Lett.* **74** 3237

[4] Ancona M G and Rendel R W 1995 *J. Appl. Phys.* **77** 393

[5] Yakimov A I, Adkins C J, Boucher R, Dvurechenskii A V, Nikiforov A I, Pchelyakov O P and Biskupski G 1999 *Phys. Rev.* B **59** 12 598

[6] Yakimov A I, Dvurechenskii A V, Prockuryakov Yu, Nikiforov A I, Pchelyakov O P, Teys S A and Gutakovskii A K 1999 *Appl. Phys. Lett.* **75** 1413

[7] Yakimov A I, Dvurechenskii A V, Nikiforov A I and Pchelyakov O P 1998 *Thin Solid Films* **336** 332

[8] Yakimov A I, Dvurechenskii A V, Nikiforov A I and Pchelyakov O P 1999 *Phys. Low-Dimens. Struct.* **3+4** (part III) 99

[9] Zhang S K, Zhu H J, Lu F, Jiang Z M and Wang Xun 1998 *Phys. Rev. Lett.* **80** 3340

[10] Beenakker C W J 1991 *Phys. Rev.* B **44** 1646

[11] Nguyen V L 1984 *Fiz. Tekh. Poluprov.* **18** 335 (Engl. Transl. 1984 *Sov. Phys.–Semicond.* **18** 207)